REMARKS/ARGUMENTS

Rejections 35 U.S.C. §102

Claims 1-3, 5-7 and 10-12 are rejected, under 35 U.S.C. §102(b), as being allegedly anticipated by Larsen et al, (US Pat No. 5,115,500) (hereinafter Larsen). Applicants respectfully traverse in view of the following.

Independent Claim 1 recites a limitation whereby a plurality of possible meanings are associated with an instruction by the same processor, as claimed. Accordingly, one instruction may have multiple attributed meanings by the same processor. Moreover, independent Claim 1 recites a limitation whereby the portion of the corresponding address determines a meaning for the extended instruction from possible meanings, as claimed. Furthermore, independent Claim 1 recites concatenating a portion of the corresponding address to the instruction to form an extended instruction, as claimed. Independent Claim 1 further recites that the concatenation, thereby increases the number of instructions in an instruction set, as claimed.

Larsen discloses that instructions in different formats are normally incompatible which may have been written for different machine types (see Larsen, Abstract). Larsen further discloses that to provide compatibility between different formats, instructions are placed in predefined areas of the instruction

store where they are fetched and decoded based on the portions of both the fetched-from address and the instruction itself (see Larsen, Abstract).

In particular Larsen discloses that an instruction store is partitioned for accommodating two types of different, incompatible format machine language instructions (see Larsen, col. 5, lines 41-44). Larsen further discloses that high order addresses have been arbitrarily reserved for machine type or format instructions (see Larsen, col. 5, lines 44-46). The effect of using the fetched-from address as part of the access specifications for decoding the specific instruction that is fetched, is to permit instructions in different regions to be decoded using different rules (see Larsen, col. 6, lines 25-30). Larsen discloses that instruction stored in different portions of the memory store are decoded differently (e.g., type 1 and type 2) based on where the instruction is stored (see Larsen, col. 6, lines 30-40). Larsen further gives an example for an "add instruction" in different formats (e.g., type 1 and type 2) that are decoded based on a portion of the location where the instruction is stored (see Larsen, col. 6 line 41 to col. 8 line 18).

Accordingly, Larsen discloses that the same instruction (e.g., "add instruction") is decoded differently such that it can be executed on different machines based on where the instruction is stored, however, each decode nevertheless leads to the same meaning, e.g., an add instruction. Thus, the

number of instructions remain unchanged since the instruction performs the same task (e.g., add) but on a different machine, having the same result (e.g., addition) . Therefore, not only Larsen fails to disclose or suggest increasing the number of instructions in an instruction set, as claimed but Larsen teaches away by disclosing that the same instruction in different locations performs the same operation (e.g., to add), thereby having the same number of instructions (e.g., both instructions for different machines perform an "add" instruction).

Importantly, as discussed and presented above Larsen discloses that an instruction stored is partitioned to accommodate different machine types with different types of machine language instructions that have incompatible formats. Thus, Larsen discloses different types of machine language instructions for different processors having incompatible formats. Therefore, Larsen fails to either teach or suggest an instruction having different meanings associated with it by the same processor, as claimed.

Furthermore, as discussed in Applicants response submitted on June 14, 2007, an instruction having different meanings, as claimed, may produce different results based on the meaning whereas an instruction having the same meaning but decoded differently produces the same result, as disclosed by Larsen. Thus, the rejection inappropriately equates the same instruction being decoded differently for different types of machine formats, as disclosed by Larsen

to the instruction having a plurality of meanings, as claimed. As such, Larsen fails to either teach or suggest a plurality of possible meanings are associated with the instruction, as claimed.

Moreover, as discussed and presented above, since Larsen fails to either teach or suggest that the same instruction has more than one meaning, as claimed, Larsen also fails to teach or suggest that the portion of the corresponding address determines a meaning for the extended instruction from the possible meanings, as claimed. In this regard, the teachings of Larsen are in stark contrast to the claimed embodiment.

Furthermore, as presented and discussed above, Larsen discloses an instruction decoding register fetching the content (e.g., instruction) from an address and sending it to the instruction decode memory (see Larsen, Figure 2, elements 1, 2 and 5). Moreover, Larsen discloses an instruction decoding selection register fetching a portion of an address that contains the instruction and sending it to the instruction decode memory (see Larsen, Figure 2, elements 2, 10 and 5). The received instruction and the portion of the address are used to lookup addresses within the instruction decode memory (see Larsen, col. 6, lines 3-5). Accordingly, Larsen discloses that the instruction decode memory uses the content of the instruction and a portion of the address containing the instruction to lookup an address of the instruction in a format compliant with the machine

language. Thus, Larsen fails to explicitly teach or suggest that a concatenating a portion of the corresponding address to the instruction forms an extended instruction, as claimed because Larsen uses the input to the instruction decode memory to lookup an address instead of concatenating and forming an extended instruction, as claimed.

Accordingly, Larsen fails to anticipate independent Claim 1, under 35 U.S.C. §102(b). Independent Claims 5 and 10 recite limitations similar to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency. As such, allowance of Claims 1-3, 5-7 and 10-12 is earnestly solicited.

Rejections 35 U.S.C. §103

Claims 4, 8-9 and 13-14 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Larsen in view of ("390 Principles of Operation") (hereinafter IBM). Applicants respectfully traverse in view of the following.

As per Claims 4, 8 and 13, the rejection admits that Larsen fails to teach that the plurality of possible meanings includes an integer type of instruction and a floating point type of instruction, as claimed. The rejection relies on IBM to remedy this failure. Applicants respectfully submit that IBM discloses a floating point format (see IBM page 9-1) such as hexadecimal floating point, binary

floating point and etc. (see IBM page 9-1). IBM further discloses general instruction types such as signed/unsigned binary integers, their representations and their arithmetic (see IBM pages 7-2 to 7-5). Accordingly, IBM explicitly discloses that each instruction has only one type (e.g., floating point, signed binary integer, unsigned binary integer). As such, IBM fails to disclose that the plurality of possible meanings includes an integer type of instruction and a floating point type of instruction, as claimed.

Moreover, IBM teaches away from the limitation wherein an instruction from a memory unit is fetched, wherein a plurality of possible meanings are associated with the instruction, as claimed. IBM discloses that all floating point instructions use the same floating point registers (see IBM page 9-2). Thus, floating point instructions and integer type instructions are stored on different registers and not on the same memory unit. Since floating point instructions and integer type instructions must be stored on separate registers, as disclosed by IBM, the instruction from a memory unit cannot have a plurality of possible meanings associated with the instruction, as claimed.

As such, allowance of Claims 4, 8 and 13 is earnestly solicited.

As per Claims 9 and 14, the rejection admits that Larsen fails to teach that generating the instruction and the storing the instruction are performed by a

compiler, as claimed. The rejection takes Official Notice that "compilers are used to generate and store instructions in memory, as to allow programmers to write code in high level languages and allow the compiler to convert and prepare the code for execution by a processor." Applicants have previously filed a response on February 2, 2007 challenging the Official Notice. The rejection asserts that "it does not appear that the applicant is requesting prior art that discloses a compiler generating and storing instructions. Thus, the Examiner has not brought in prior art to teach this limitation and maintains that claim 9 is obvious in light of the official notice given."

Applicants respectfully remind the Examiner that to adequately traverse an Official Notice an Applicant must specifically point out the supposed errors in the Examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art (see 37 CFR 1.111(b) and MPEP 2144.03(C)). If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained (see 37 CFR 1.104(c)(2) and MPEP 2144.03(C)). Accordingly, Applicants respectfully submit that since the Applicant adequately traversed the Official Notice in the response filed on February 2, 2007, the rejection must provide documentary evidence in the current Office Action regardless of an explicit request from the Applicants. As

such, withdrawal of this rejection based on the Official Notice is earnestly solicited.

As such, allowance of Claims 9 and 14 is earnestly requested.

For the above reasons, the Applicants request reconsideration and withdrawal of the objections and rejections of record.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-14 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-14 are in condition for allowance.

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Respectfully submitted,
MURABITO, HAO & BARNES LLP

Amir A. Tabarrok
Registration No. 57,137

MURABITO, HAO & BARNES LLP
Two North Market Street
Third Floor
San Jose, California 95113

(408) 938-9060 Voice
(408) 938-9069 Facsimile